AMENDMENTS IN THE SPECIFICATION

Please replace the paragraph beginning on page 12, line 20 with the following:

Figure 3 provides a first and second generation heterogeneous upgrade, with each generation represented by a different processor and cache topology.   As illustrated, processor C **301c** and processor D **301D** each operate at a different frequency. Each processor is connected via interconnect **316,** which may also operate at a different frequency. Because of the frequency differences possible in the processor and cache hardware models all connected to an interconnect **316** with a set frequency, the processing system's communication protocols are enhanced to support different ratios of frequency. Thus, the frequency ratios between the processors, the caches, and the interconnect **316** is N:M, where N and M may be different integers. For example, the frequency ratios may be 2:1, 3:1, 4:1, 5:2, 7:4, etc. The second generation upgrade heterogeneous system illustrated in **Figure 3** provides a 2:1, 3:1, 4:1 ratio with the regards to the processor frequencies versus the frequency of interconnect **316**. As illustrated, interconnect **316** operates at 250 megahertz (MHz), processor A **310a** and processor B **310b** operate at a 500 megahertz frequency, and processor C **310c** and processor D **310d** operate at 2 gigahertz (GHz) and 3 Ghz, respectively. Of course, the processor frequency may be asynchronous with the interconnect's frequency whereby no whole number ratio can be attributed.

Please replace the paragraph beginning on page 17, line 3 with the following:

As each new processor is added to the data processing system, the system logs information about the new processor including the processor's operational characteristics, cache topologies, etc., which is then utilized during operation to enable correct interactions with other components and more efficient processing, i.e., sharing and allocation of work among processors. An evaluation of the data processing system may be performed by operating system **24,** which then provides [[a]] system centric enhancements related to cache intervention, prefetching, intelligent cache states, etc., in order to optimize the results of these operations.

Please replace the paragraph beginning on page 19, line 3 with the following:

When a read (address) is issued by the extended processor **610c,** the master select pin for that processor is activated. The other extended processor **610d** snoops the read transaction and

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recognizes that the master is also an extended processor because of the activated master select pin **616c**. Knowing that the master is extended, the other extended processor **610d**, which is in the R cache state, drives the extended snoop response bus **616e** with shared intervention information. Also, extended the snooper (extended processor **610d**) sends a snoop retry on base snoop response bus **616d**. The master then consumes the shared intervention data from the other extended processor and moves from I to R state. The extended snooper then moves from R to S state.

Please amend the abstract as follows:

~~SYMMETRIC MULTIPROCESSING (SMP) SYSTEM WITH FULLY-INTERCONNECTED HETEROGENOUS MICROPROCESSORS~~

Disclosed is a fully-interconnected, heterogenous, multiprocessor data processing system. The data processing system topology has a plurality of processors each having unique characteristics including, for example, different processing speeds (frequency), different integrated circuit design, different cache topologies (sizes, levels, etc.). The processors are interconnected via a system bus or switch and communicate via an enhanced communication protocol that supports the heterogeneous topology and enables each processor to process data and operate at their respective frequencies. Second and third generation heterogenous processors are connected to a specialized set of pins, connected to the system bus that allow the newer processors to support enhanced system bus protocols with downward compatibility to the previous generation processors. Various processor functions are modified to support operations on either of the processors depending on which processor is assigned which operations. The enhanced communication protocol, operating system, and other processor logic enable the heterogenous multiprocessor data processing system to operate as a symmetric multiprocessor system.